

**ST. ANN'S COLLEGE OF ENGINEERING & TECHNOLOGY: CHIRALA**  
**DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING**  
**LECTURE SCHEDULE**

**Subject : Digital Logic Design**

**SEC-B**

**Name: S.SAI SANDEEP**

**Year & SEM /Section: II-I SEM**

**No. of Lectures per week : 4+1**

**Academic Year: 2017-18**

S.NO	DATE	UNIT. No	TOPICS
1.	12-06-2017	<b>UNIT-I</b>	<b>Unit 1</b> Introduction :Digital Systems and Binary Numbers
2.	13-06-2017		Binary, Octal, Decimal, Hexadecimal number systems
3.	14-06-2017		Conversion Of Numbers From One Radix To Another Radix
4.	15-06-2017		Conversion Of Numbers From One Radix To Another Radix
5.	17-06-2017		R's Complement And (R-1)'S Complement
6.	19-06-2017		Complement Subtraction Of Unsigned Numbers
7.	20-06-2017		Tutorial
8.	21-06-2017		Signed Binary Numbers
9.	22-06-2017		Weighted And Non Weighted Codes
10.	24-06-2017		PPT on UNIT-I
11.	27-06-2017		Tutorial
12.	28-06-2017		NPTEL VIDEO
13.	29-06-2017		EXAM ON UNIT -1
14.	01-07-2017	<b>UNIT-II</b>	<b>Unit –II</b> Introduction : Concept of Boolean Algebra
15.	03-07-2017		Boolean laws and theorems,complement and dual of logic expressions
16.	04-07-2017		Tutorial
17.	05-07-2017		Basic gates Not,And,Or,universal gates ex-or and ex-nor gates
18.	06-07-2017		Minimizations of logic gates using universal gates
19.	10-07-2017		Sop & Pos minimizations of logic functions using Boolean algebra
20.	11-07-2017		Tutorial
21.	12-07-2017		Two level realization of logic gates using universal gates
22.	13-07-2017		PPT ON UNIT-II
23.	15-07-2017		NPTEL VIDEO
24.	17-07-2017		EXAM ON UNIT -II

25.	18-07-2017		Tutorial	
26.	19-07-2017	<b>UNIT -III</b>	<b>UNIT –III</b> Introduction : Gate – Level Minimization Karnaugh map method (k-map);minimization of Boolean functions maximum using 2,3,4 variable map	
27.	20-07-2017		Karnaugh map method (k-map);minimization of Boolean functions maximum using 2,3,4 variable map	
28.	22-07-2017		Pos and sop ,simplifications with don't case conditions using k-map	
29.	24-07-2017		Pos and sop ,simplifications with don't case conditions using k-map	
30.	25-07-2017		Tutorial	
31.	26-07-2017		Nand and Nor implementation	
32.	27-07-2017		Problems	
33.	29-07-2017		PPT ON UNIT-III	
34.	31-07-2017		EXAM ON UNIT-III	
35.	01-08-2017		Tutorial	
36.	02-08-2017		<b>UNIT- IV</b>	<b>Unit –IV</b> Introduction: Combinational Logic :Design of half adder and full adder
37.	03-08-2017			Ripple adder and subtractor using ones and twos complement method
38.	05-08-2017			Design of half sub tractor and full sub tractor
39.	07-08-2017			MID EXAM-I
40.	08-08-2017	MID EXAM-I		
41.	09-08-2017	MID EXAM-I		
42.	10-08-2017	MID EXAM-I		
43.	12-08-2017	MID EXAM-I		
44.	16-08-2017	Tutorial		
45.	17-08-2017	Design of decoders and encoders ,Design of multiplexers and demultiplexers		
46.	19-08-2017	Problems		
47.	21-08-2017	HDL models of sequential circuits		
48.	22-08-2017	Tutorial		
49.	23-08-2017	Design of sequential circuits		
50.	24-08-2017	PPT ON UNIT-I		
51.	28-08-2017	NPTEL VIDEO		

52.	29-08-2017		Tutorial	
53.	30-08-2017	<b>UNIT-V</b>	<b>Unit –V</b> Introduction:synchronous sequential logic	
54.	31-08-2017		Classifications of sequential circuits, basic sequential logic circuits	
55.	04-09-2017		Latch and flip flop, RS latch using NAND gate and nor gates and truth tables	
56.	05-09-2017		Tutorial	
57.	06-09-2017		Rs and JK flip flops and T and d flip flops	
58.	07-09-2017		Truth tables and excitation tables of flip flops	
59.	09-09-2017		Conversion of one flipflop to another flipflop	
60.	11-09-2017		Flipflops with asynchronous inputs (preset, clear)	
61.	12-09-2017		Tutorial	
62.	13-09-2017		Mealy and moore models of finite state machine	
63.	14-09-2017		PPT ON UNIT-IV	
64.	16-09-2017		EXAM ON UNIT-V	
65.	18-09-2017		<b>UNIT-VI</b>	<b>UNIT –VI:</b> Introduction :Registers And Counters
66.	19-09-2017			Tutorial
67.	20-09-2017	Control Buffer Registers		
68.	21-09-2017	Bidirectional shift registers, Universal shift registers		
69.	23-09-2017	Design of ripple counters		
70.	25-09-2017	Synchronous counters and variable modulus counters		
71.	26-09-2017	Tutorial		
72.	27-09-2017	Ring and jhonson counter		
73.	03-09-2017	Synchronous up counter		
74.	04-09-2017	Ssynchronous down counter		
75.	05-10-2017	Problems on counters		
76.	07-10-2017	Problems		
77.	09-10-2017	MIDEXAM-II		
78.	10-10-2017	MIDEXAM -II		
79.	11-10-2017	MIDEXAM-II		
80.	13-10-2017	MIDEXAM -II		
81.	14-10-2017	MIDEXAM -II		

**TEXT BOOKS:**

1. DIGITAL DESIGN , 4/E.M.MORRIS MANO ,MICHAEL D CLIETTI,PEA
2. FUNDAMENTALS OF LOGIC DESIGN , 5/E ,ROTH ,CENGAGE

**REFERENCE BOOKS:**

1. SWITCHING AND FINITE AUTOMATA THEORY, 3/E, KOHAVI, CAMBRIDGE
2. DIGITAL LOGIC DESIGN, LEACH, MALVINO, SAHA, TMH
3. MODERN DIGITAL ELECTRONICS, R.P. JAIN, TMH

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